More bits, circuits, adders (From the last class)

CS 2130: Computer Systems and Organization 1

Xinyao Yi Ph.D.
Assistant Professor

UNIVERSITY of VIRGINIA | ENGINEERING

Announcements

- Homework 1 due Monday

Adder

Can we use this in parallel to add multi-bit numbers?

What is missing?

Consider:

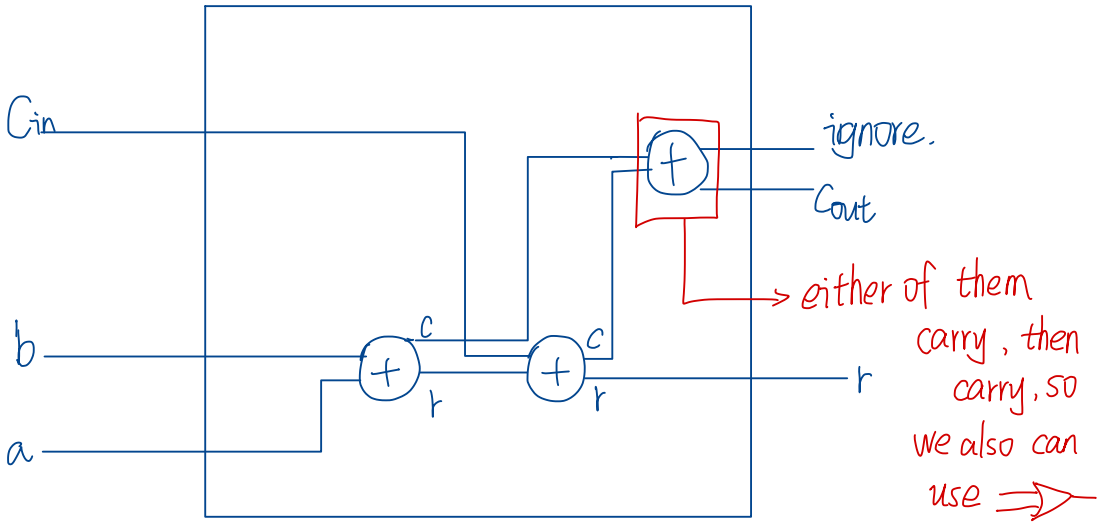
```
 '11
+01
----
 100
```

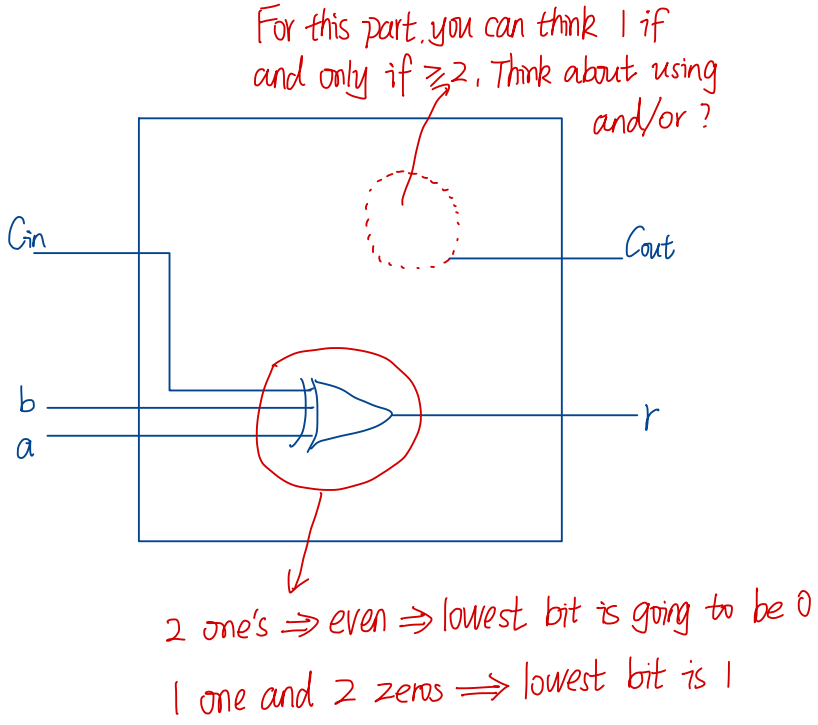
Since I have a carry-in

2 inputs → 3-inputs adder.

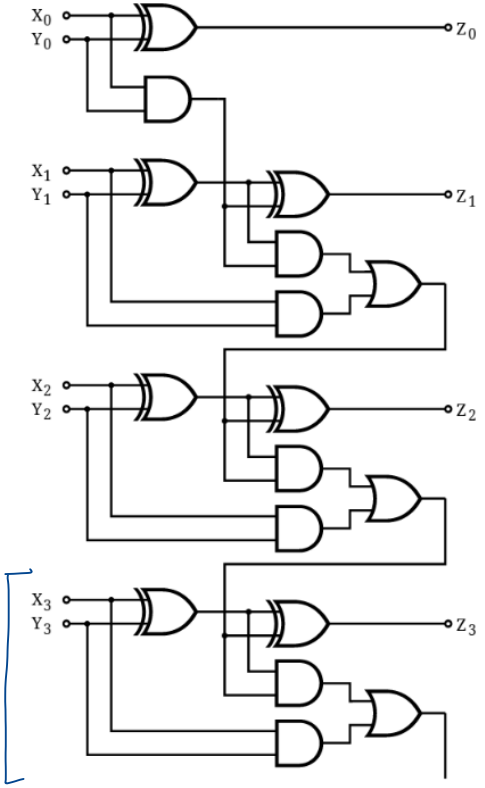
3-input Adder

Add 3 1-bit numbers: a, b, c





Ripple-Carry Adder



$X_3\ X_2\ X_1\ X_0$
$+\ Y_3\ Y_2\ Y_1\ Y_0$
$Z_3\ Z_2\ Z_1\ Z_0$

repeat if more bits

verify:

unsigned:

```
  1 1 1 1  (15)
+ 1 1 1 1  (15)
-----------
  1 1 1 0  (14)
```

drop ← (1)

overflow!

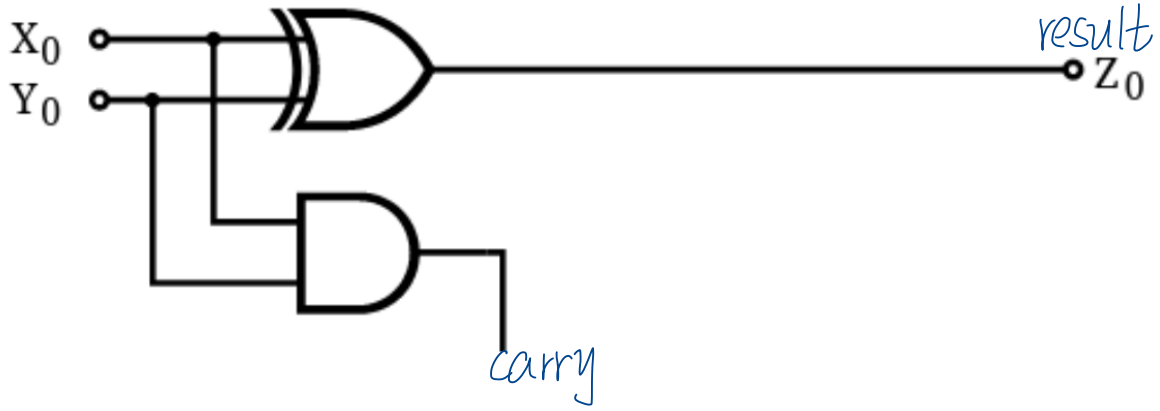
signed?

```
  1 1 1 1  (-1)
+ 1 1 1 1  (-1)
-----------
  1 1 1 0  (-2)
```

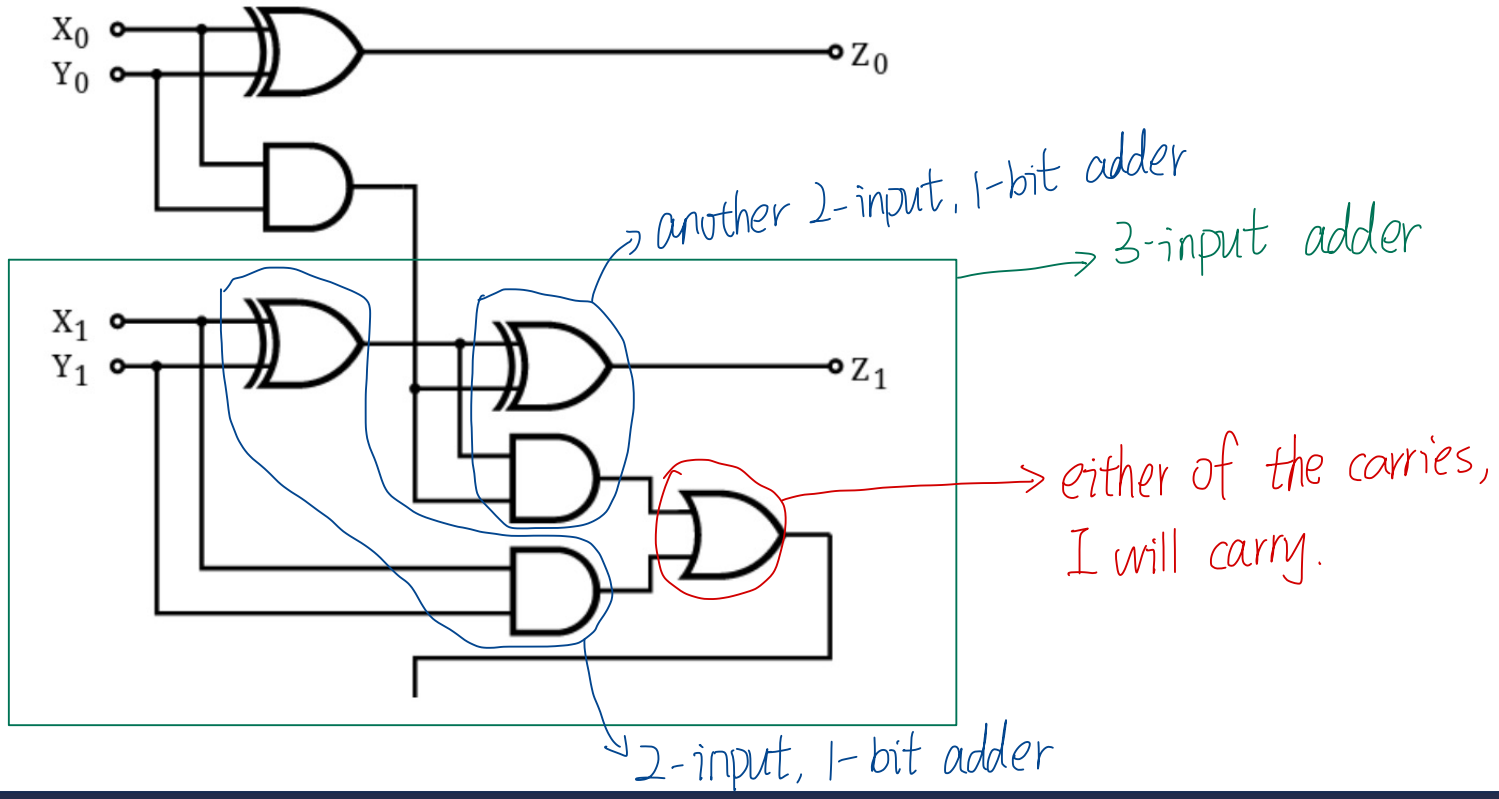
works!

Ripple-Carry Adder: Lowest-order Bit

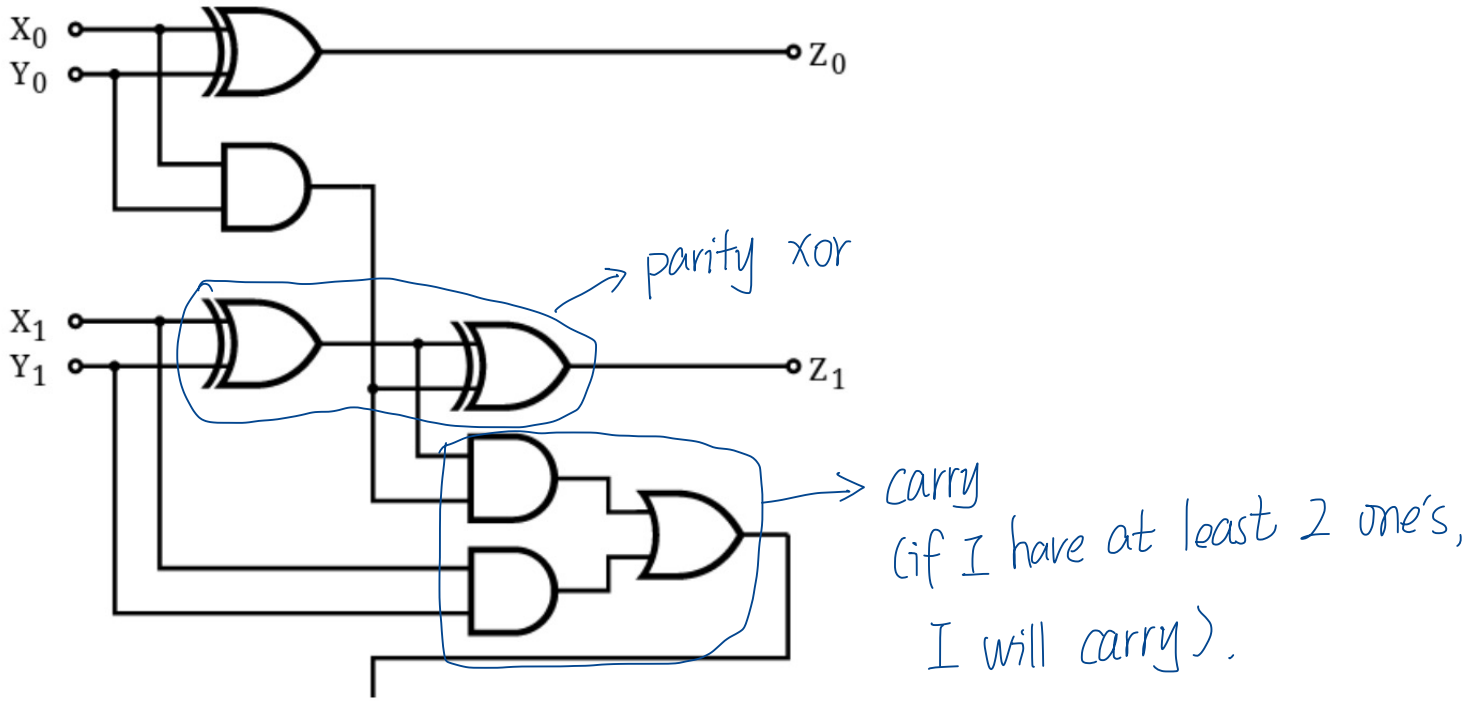
(one bit, 2 inputs adder)



Ripple-Carry Adder: In General



Ripple-Carry Adder: In General



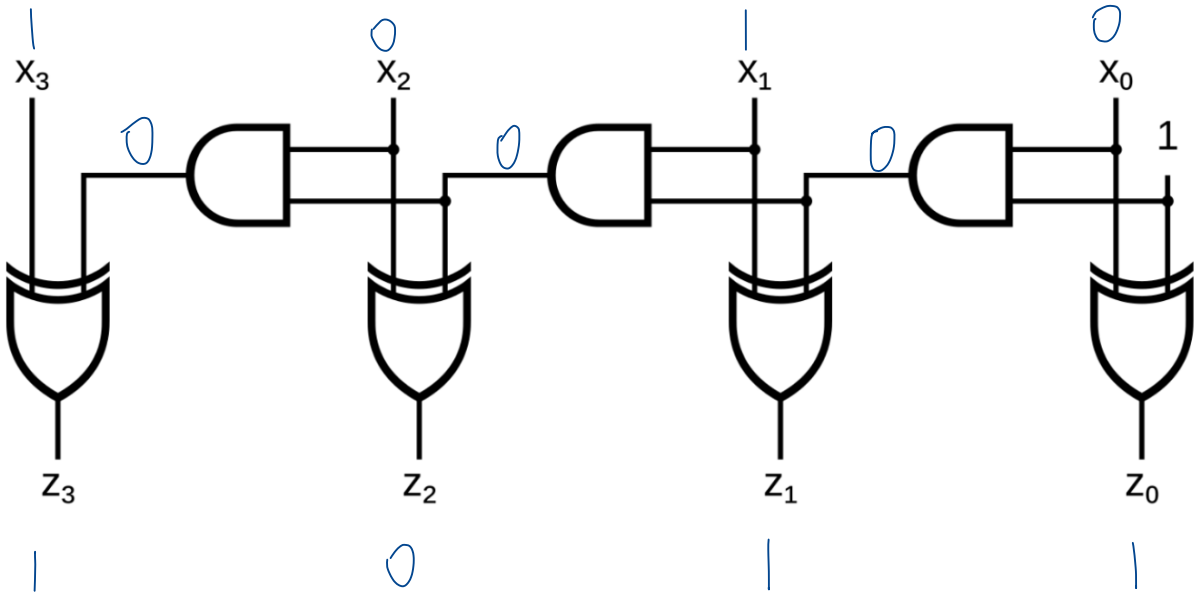
Clocks, Registers

CS 2130: Computer Systems and Organization 1

Xinyao Yi Ph.D.
Assistant Professor

UNIVERSITY of VIRGINIA | ENGINEERING

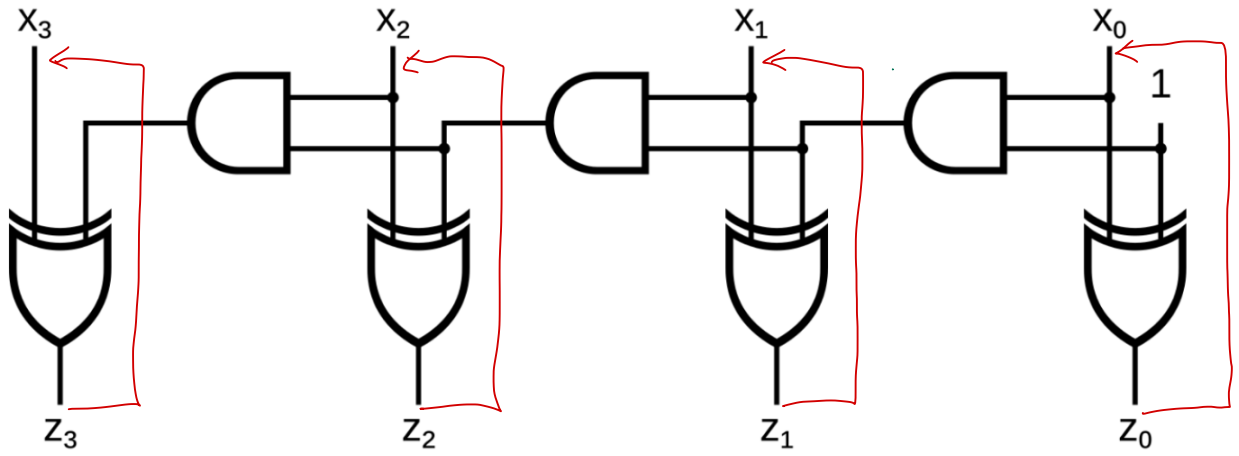
What does this circuit do?



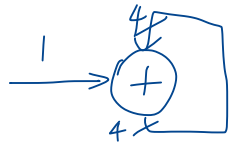
It adds 1 !

Increment Circuit

I want a counter.



Idea:



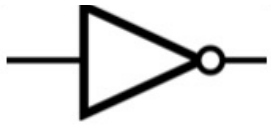
out put a one, then feed itself back, then I can count.

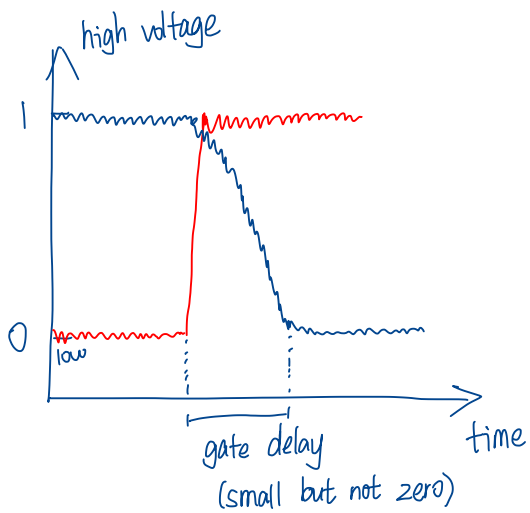
glitch happens!

I want to remember the current value.
use it as the input for the next calculation.

Gate Delay

What happens when I change my input?



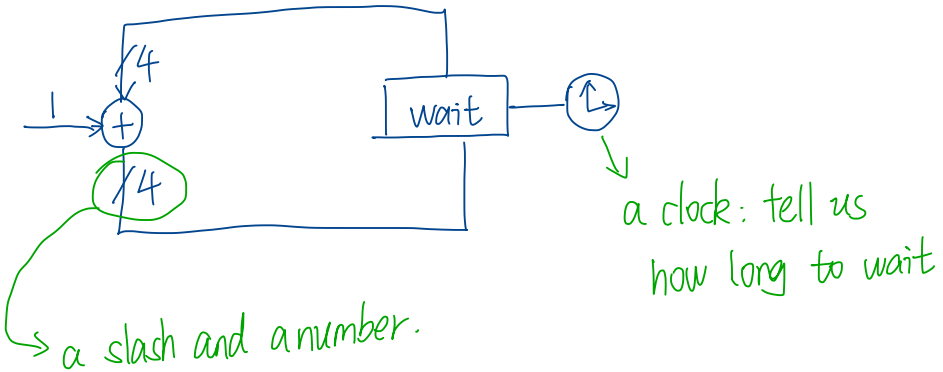


My input could change instantly.

but the output does not!

Building a Counter

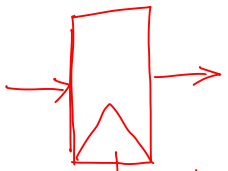
So what we want to do:



a clock: tell us how long to wait

a slash and a number.
⇓
a bundle of wires
⇓
no need to draw all wires

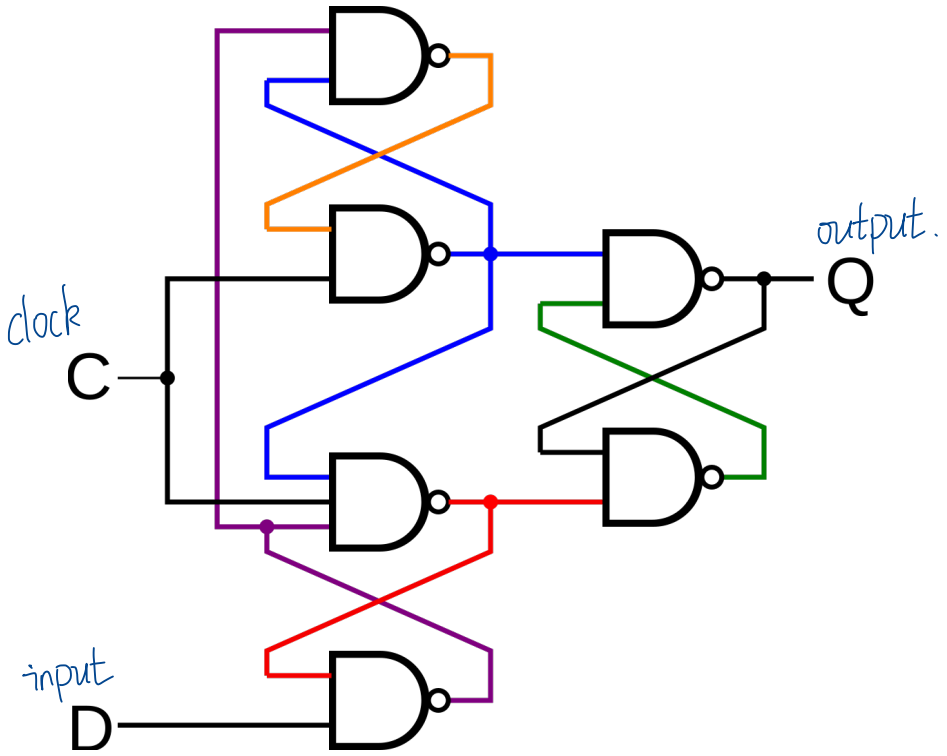
a register:

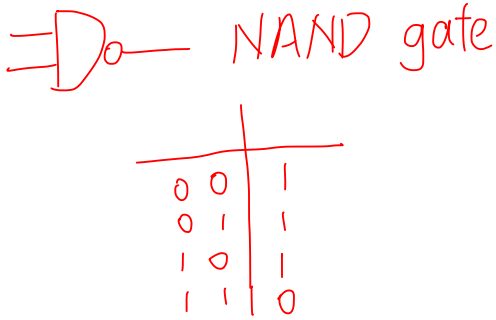


It is a memory element.

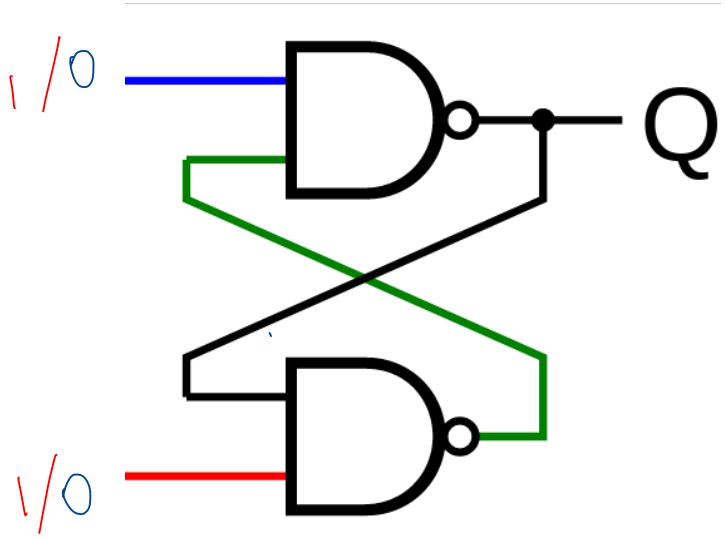
This triangle is the symbol of a clock.

1-bit Register Circuit





1-bit Register Circuit

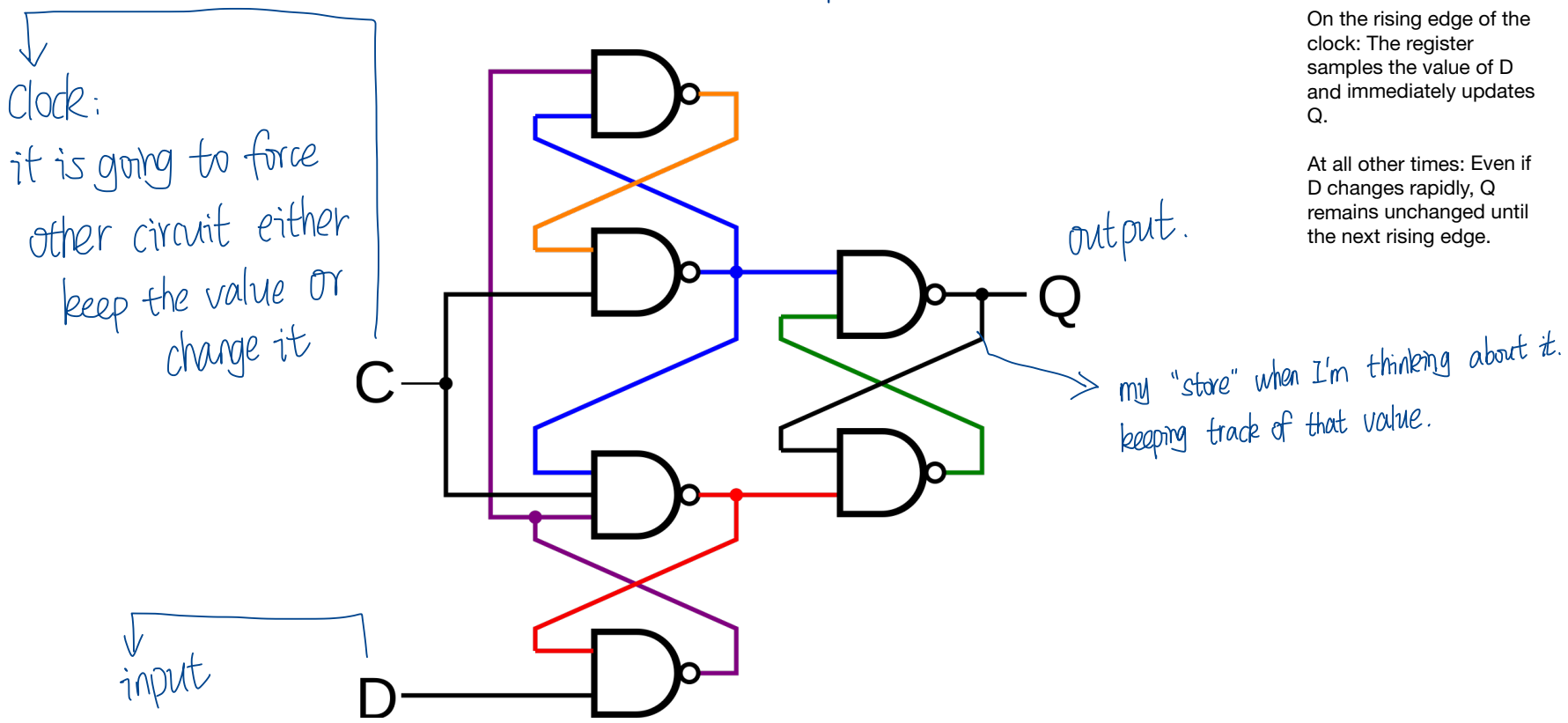


if my inputs are zeros:
make Q change from 0→1
or keep 1.

if my inputs are ones:
stay the values.

1-bit Register Circuit

D-flip-flop.

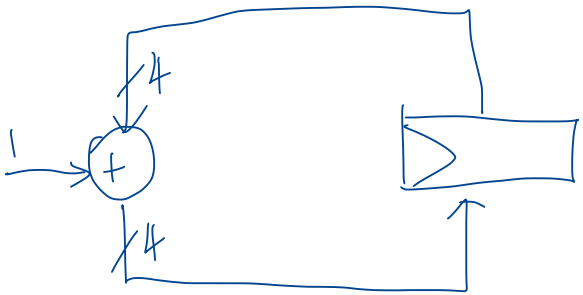


When the clock is low: The register monitors the input D, but it does not immediately update Q.

On the rising edge of the clock: The register samples the value of D and immediately updates Q.

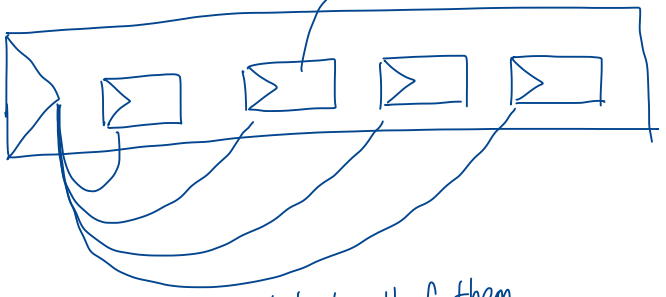
At all other times: Even if D changes rapidly, Q remains unchanged until the next rising edge.

Building a Counter



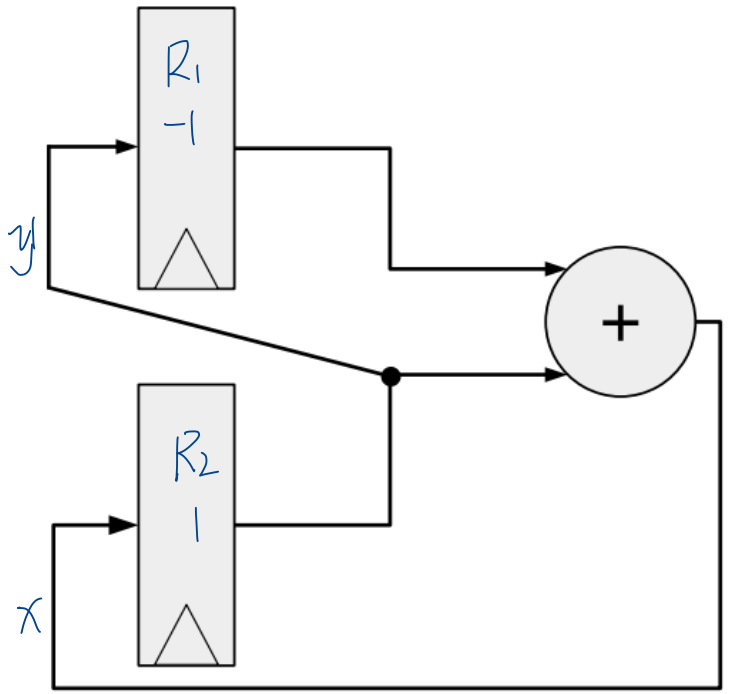
four-bit register:

four little ones for one-bit registers.



attach the clock to all of them.
they all have the same clock.

Another Counter



clock	R_1	R_2	x	y
0	-1	1	0	1
1	1	0	1	0
2	0	1	1	1
3	1	1	2	1
4	1	2	3	2
5			5	3

x : Fibonacci Sequence.

Another Counter