More bits, circuits, adders (From the last class)

CS 2130: Computer Systems and Organization 1

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Announcements

- Quiz 2 out later today, due Sunday at 11:59pm
- Homework 1 due Monday
- Homework 2 available Monday

Adder

Can we use this in parallel to add multi-bit numbers?

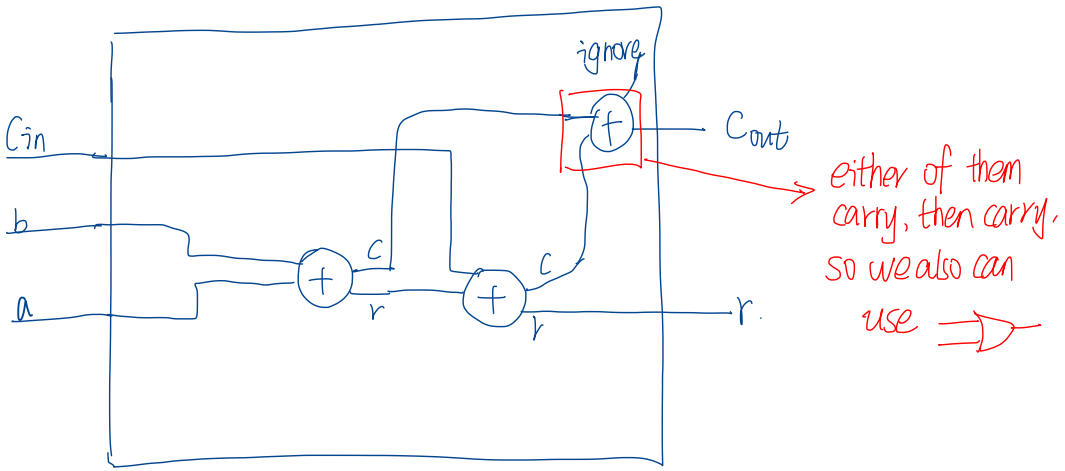
What is missing?

Consider:

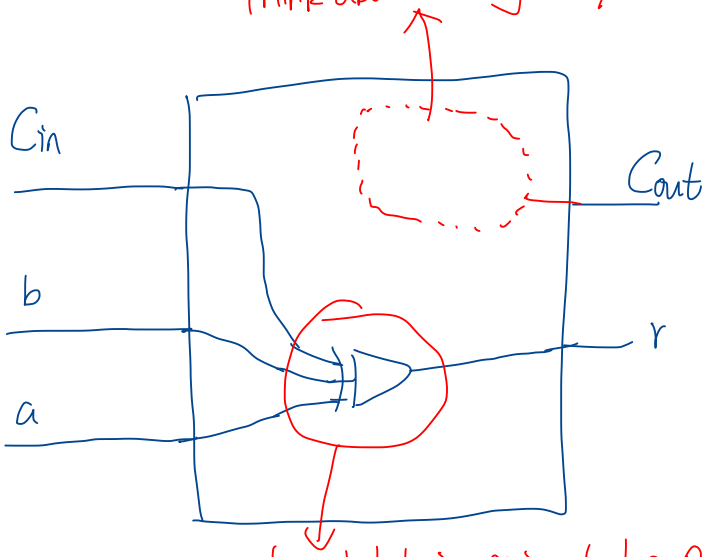
```
  11
+01
----
```

3-input Adder

Add 3 1-bit numbers: a, b, c



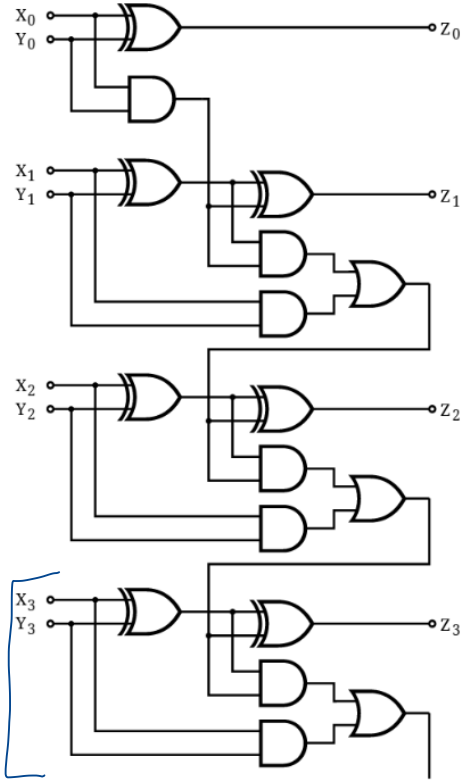
for this part, you can think:
1 if and only if ≥2.
Think about using and/or ?



2 ones ⇒ even ⇒ lowest bit is going to be 0
1 one and 2 zeros ⇒ lowest bit: 1

Ripple-Carry Adder

$X_3\ X_2\ X_1\ X_0$
$+\ Y_3\ Y_2\ Y_1\ Y_0$
$Z_3\ Z_2\ Z_1\ Z_0$



repeat if more bits

verify:

unsigned?

```
  1 1 1 1   (15)
+ 1 1 1 1   (15)
-----------
1 1 1 1 0   (14)
```

drop ← (1)

overflow!

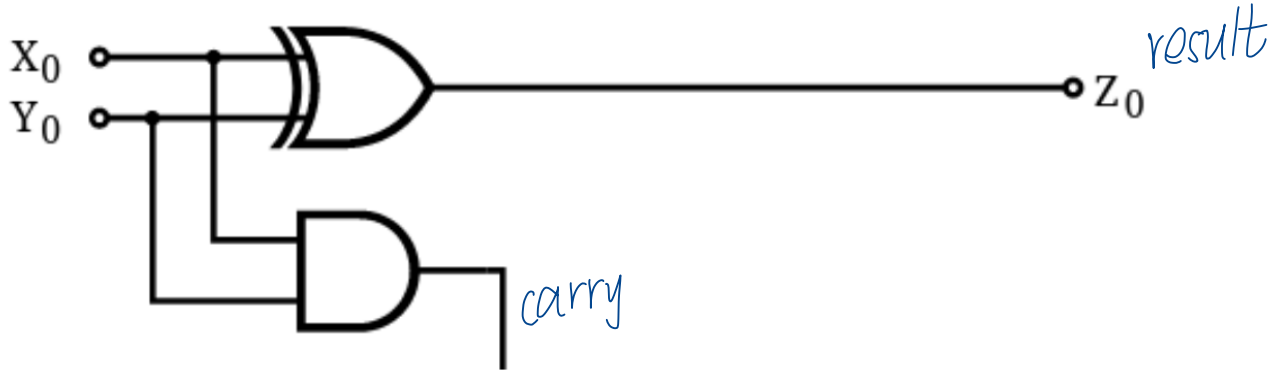
signed?

```
  1 1 1 1   (-1)
+ 1 1 1 1   (-1)
-----------
1 1 1 1 0   (-2)
```

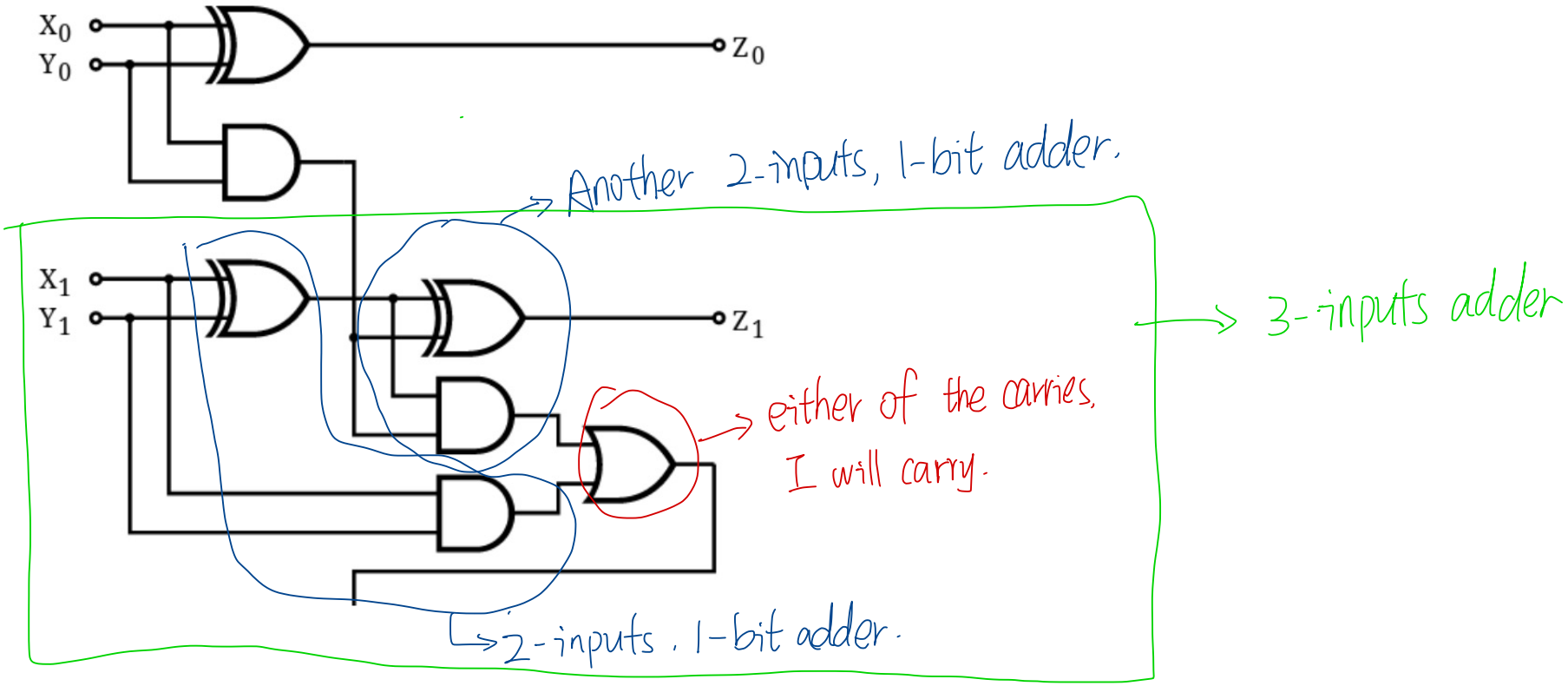
works!

Ripple-Carry Adder: Lowest-order Bit

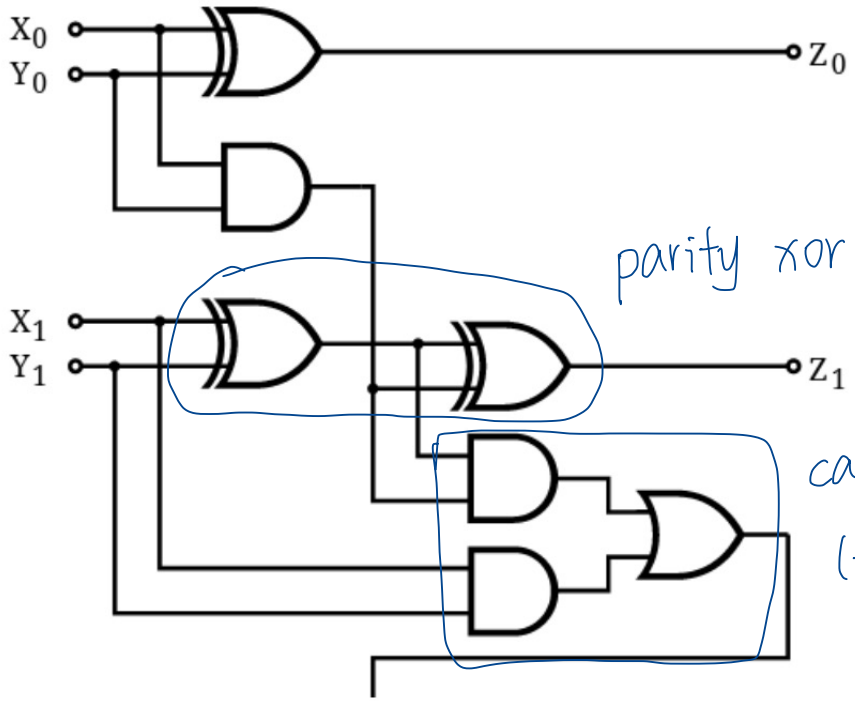
(one bit 2 inputs adder)



Ripple-Carry Adder: In General



Ripple-Carry Adder: In General



Clocks, Registers

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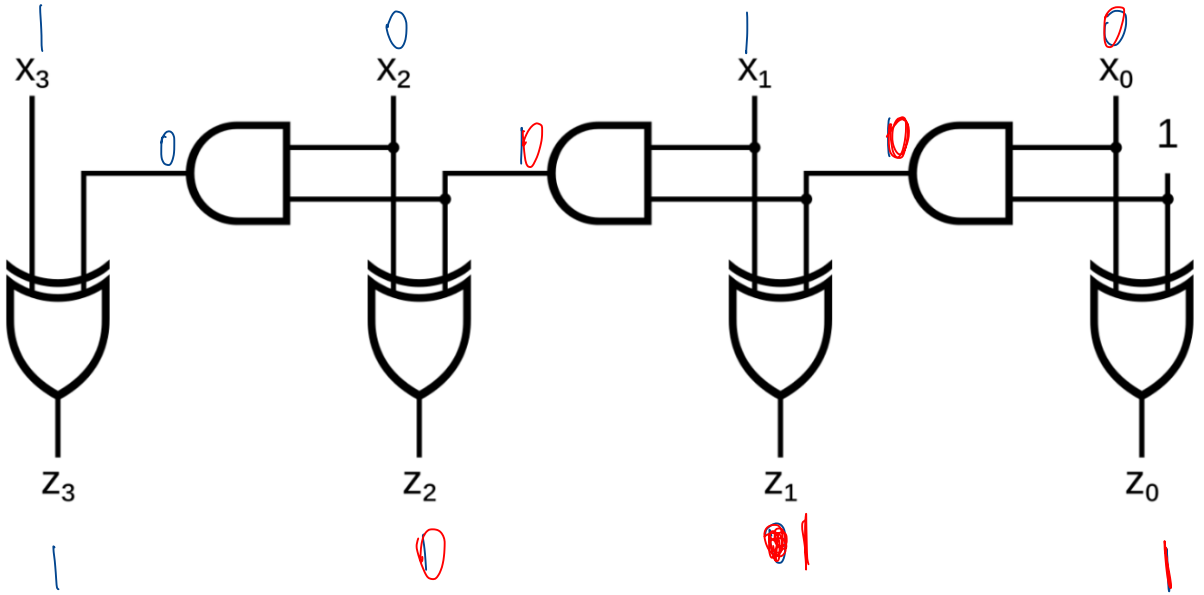
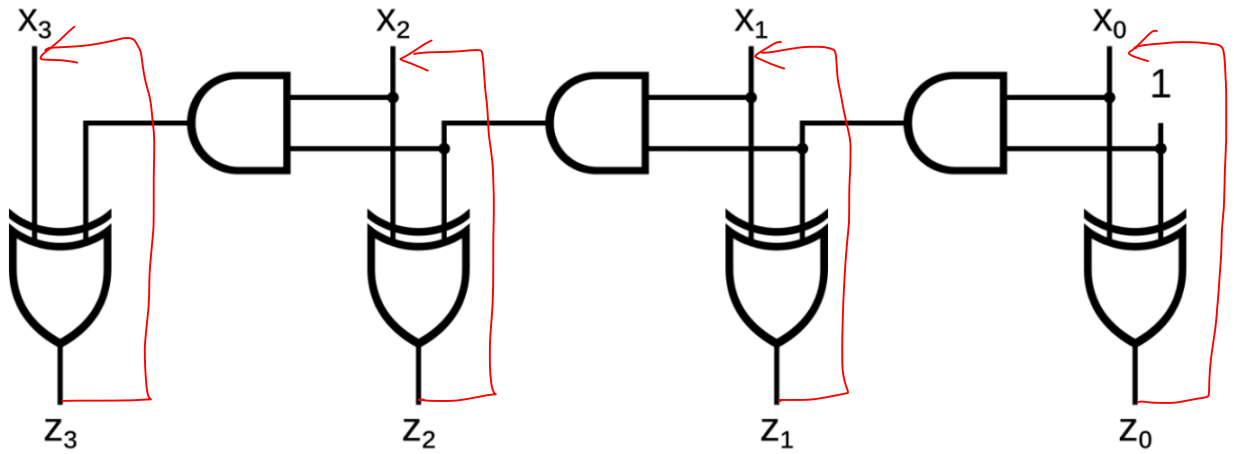
What does this circuit do?



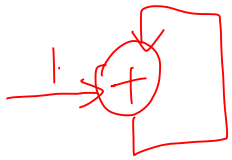
It add 1 !

Increment Circuit

I want a counter.



Idea:

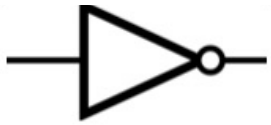


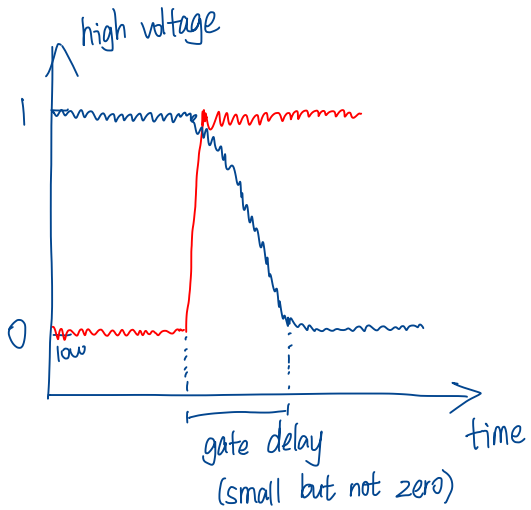
output a one, then feed itself back, then I can count.

but glitch happens!

Gate Delay

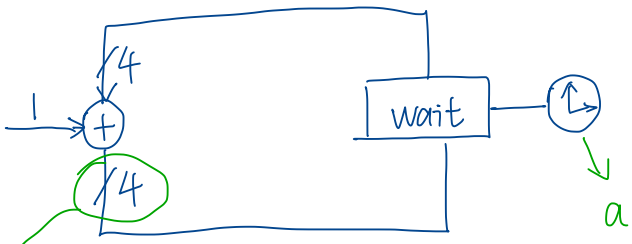
What happens when I change my input?





Building a Counter

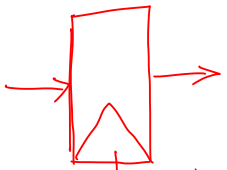
So what we want to do:



a clock: tell us how long to wait

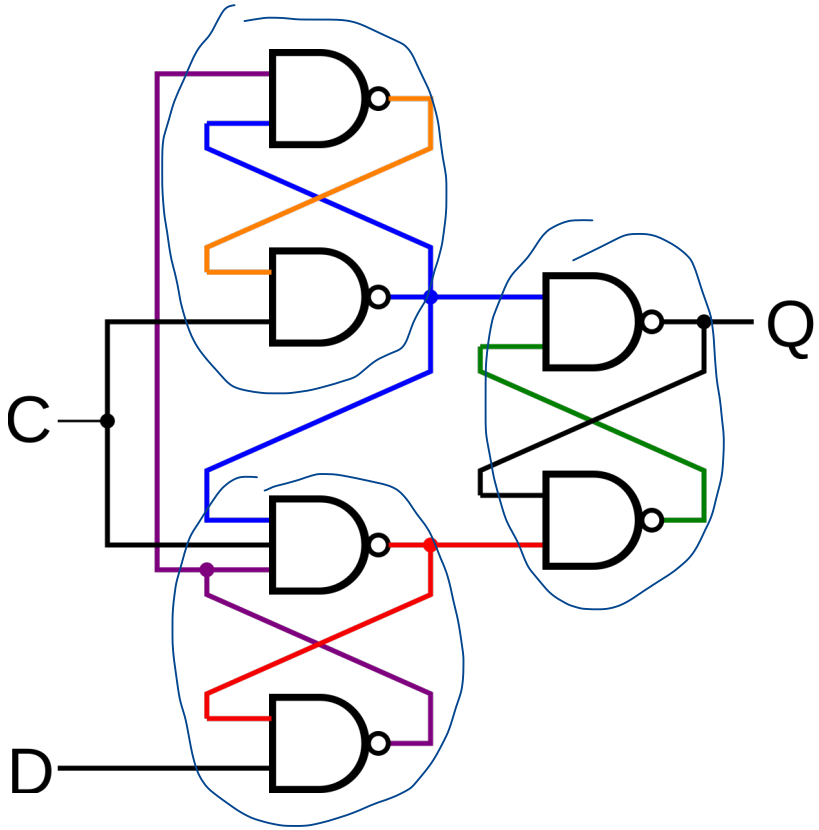
a slash and a number.
⇓
a bundle of wires
⇓
no need to draw all wires

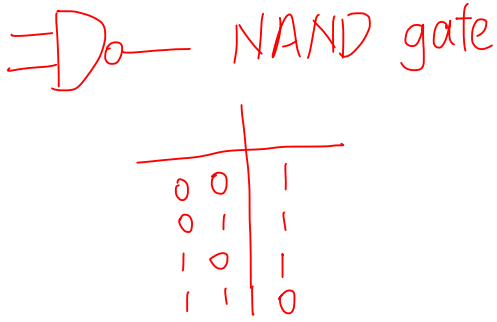
a register:



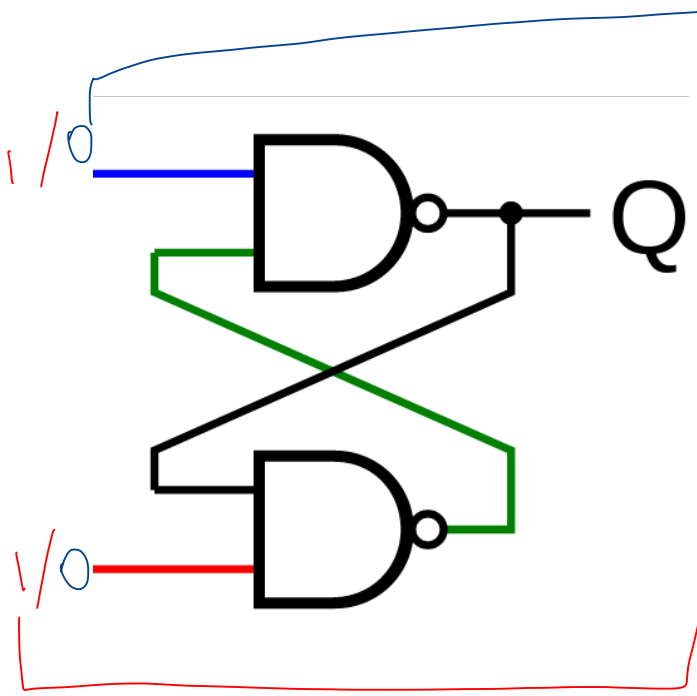
This triangle is the symbol of a clock.

1-bit Register Circuit





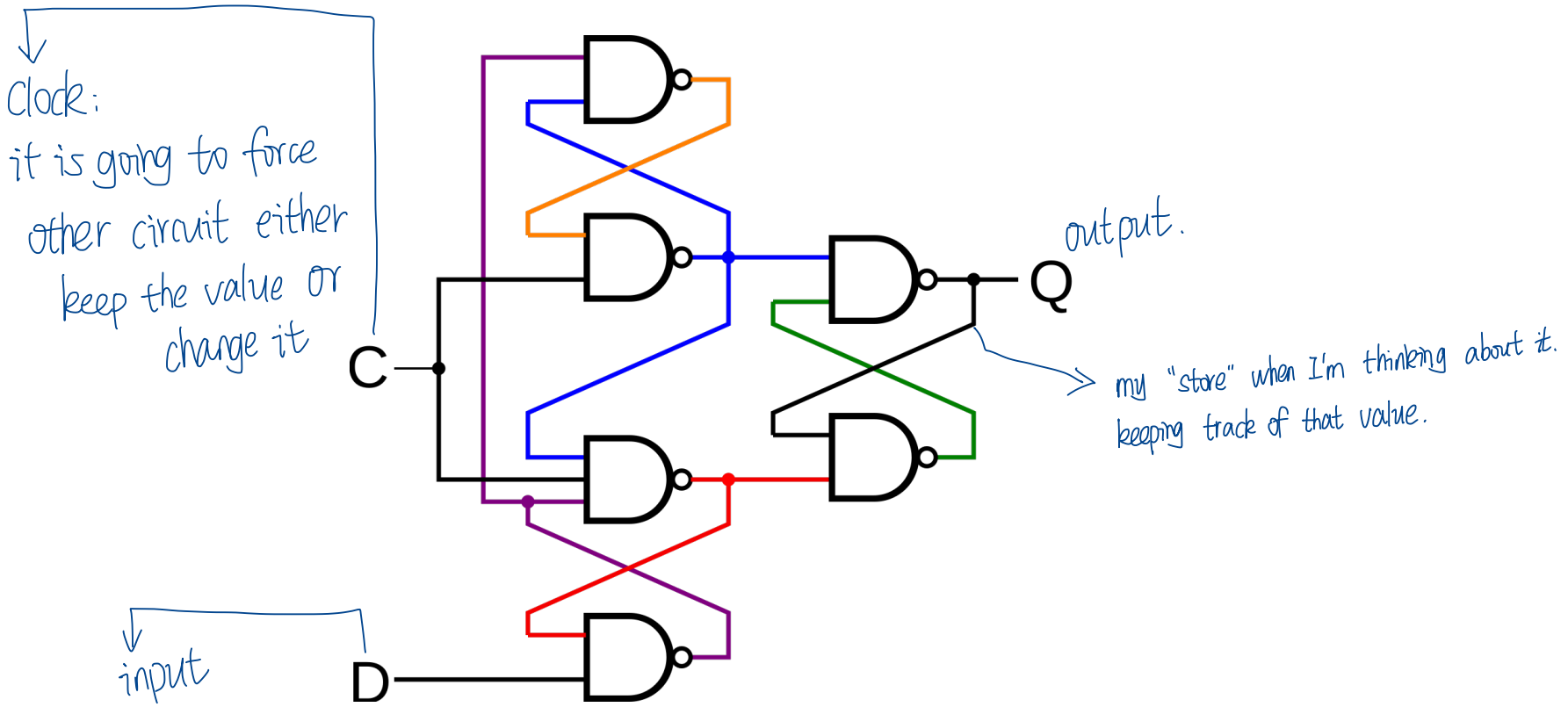
1-bit Register Circuit



if my inputs are zeros:
make Q change from 0→1
or keep 1.

if my inputs are ones:
stay the values.

1-bit Register Circuit

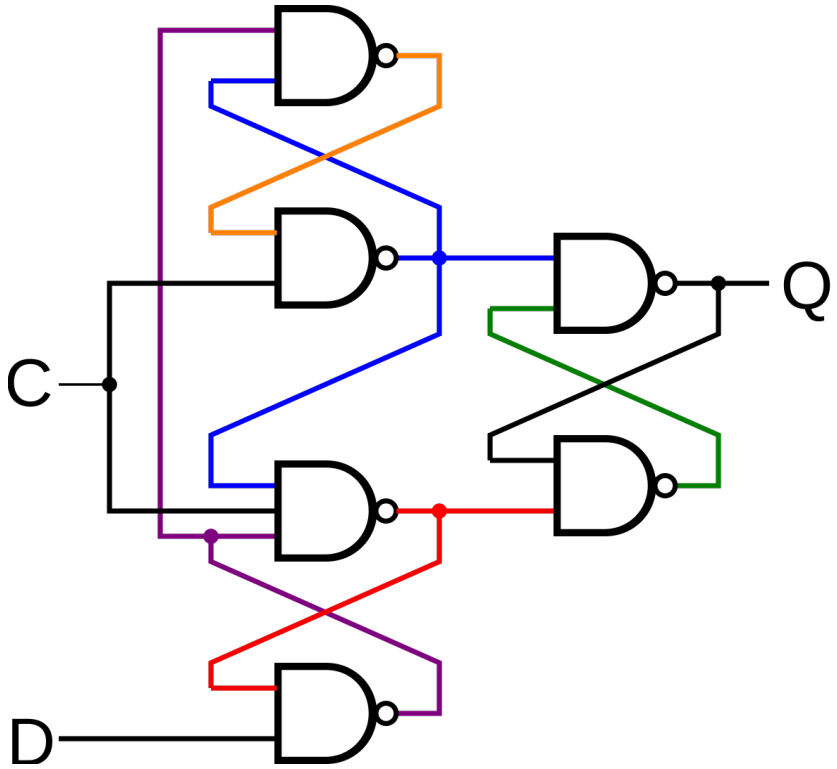


1-bit Register Circuit

When the clock is low: The register monitors the input D, but it does not immediately update Q.

On the rising edge of the clock: The register samples the value of D and immediately updates Q.

At all other times: Even if D changes rapidly, Q remains unchanged until the next rising edge.



Building a Counter

four-bit register: